

CUST#069002  
 NPO#EME-F0021-USA-1/柯嘉初桃/柯耀琦

# REMARKS

Claim 12 is objected to under 37 CFR 1.75(c). Claims 9-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as invention. Claims 1-2, 5-6 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Onakado et al., U.S. Patent 6,107,659 in view of Bergemont, U.S. Patent 5,409,854 and further in view of Komori et al., U.S. Patent 5,352,620. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Onakado et al., U.S. Patent 6,107,659 in view of Bergemont, U.S. Patent 5,409,854 and further in view of Komori et al., U.S. Patent 5,352,620, and further in view of Hsieh et al., U.S. Patent 6,204,126.

## 1. Objection to the claim 12 under 37 CFR 1.75(c):

Claim 12 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in dependent form. Claim 12 does not have all the limitations of the dependent claim because it teaches replacing limitations of the independent claim(s) and substituting them with other limitations.

## 30 Response:

Claim 12 has been deleted to overcome the objection under 37 CFR 1.75(c). No new matter is entered.

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Allowance of the present application is politely requested.

**2. Rejection of claims 9-12 under 35 U.S.C. 112:**

- 5        Claim 9 lacks antecedent basis for "said n-type region implanted...". Clarification is required. No prior art rejection is made on these claims because the scope of the claims cannot be determined.

10    **Response:**

- As specified in the above AMENDMENTS TO THE CLAIMS section, claim 9 is amended to be dependent upon the amended claim 1, thereby rendering claim 9 definite. No new matter is entered. Allowance of the amended claim  
 15    9 is hereby requested.

**3. Ownership:**

- This application currently names joint inventors. In considering patentability of the claims under 35  
 20    U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor  
 25    and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f), or (g) prior art under 35 U.S.C. 103(a).

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**Response:**

      All of the claims in the present application are

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commonly own d.

4. Rejection of claims 1-2, 5-6, and 13-16 under 35 U.S.C. 103(a):

- 5 Onkado et al. shows the invention substantially as claimed s structure of an embedded channel write/ erase flash memory cell comprising: an n-type silicon substrate; a flash memory cell region comprising mainly: a deep P-well formed on in said substrate; an N-well  
10 formed on in said deep P-well; a stacked gate formed on said N-well; and associated peripheral transistor circuitry (see fig.42 and col.24-lines 33-55).

- 15 Onkado et al. fail to expressly disclose the peripheral transistors formed in a triple well and a shallow and a deep p-type region formed in the N-well of the flash memory cell.

- 20 Bergemont discloses forming both the peripheral and memory circuitry of a nonvolatile memory device in triple wells (see fig.2B and col.4-lines 52-57). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Onkado  
25 et al. so as to have both the peripheral and memory arrays formed in triple well because this provides increased breakdown voltage protection for both the memory and peripheral circuits.

- 30 Komori et al. discloses forming both deep and shallow regions in a memory cell region of an opposite conductivity type to the substrate in order to improve

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the reading and writing of the memory cell (see col.2-lin s 46-63 and fig.3). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of Onkado et al. modified by Bergemont so as to form a shallow and deep p-type region in the n-well of the memory cell because this would allow for the formation of a highly efficient p-type flash memory.

10 **Response:**

The amended claim 1 is amended through emerging claims 4 and 7 into claim 1. No new matter is introduced. The amended claim 1 of the present application is repeated below:

15

"1. A structure of an embedded channel write/erase flash memory cell, comprising mainly:

an N-substrate;

a flash memory cell region comprising mainly:

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a deep P-well formed in said substrate;

an N-well formed in said deep P-well, a deep p-type region and a shallow p-type region being implanted in predetermined positions of said N-well;

25

a first n-type region formed at one side of said shallow p-type region and in said deep p-type region in said N-well to be used as a drain;

a second n-type region formed at the other side of said shallow p-type region in said N-well to be used as a source; and

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a stacked gate formed on said N-well; and

a CMOS device region comprising mainly:

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a first deep P-well formed in said substrat ;  
 a first N-well formed in said first deep P-well,  
 a plurality of p-type regions being implanted  
 in predetermined positions of said first  
 5 N-well;  
 a second deep P-well formed in said substrate;  
 and  
 a second N-well formed in said second deep P-well,  
 a plurality of p-type regions being implanted  
 10 in predetermined positions of said second  
 N-well."

As described in the amended claim 1 and Fig. 1T, a  
 first n-type region 17 to be used as a drain is formed  
 15 at one side of the said shallow p-type region 15 and  
 in said deep p-type region 12 in said N-well 14, and  
 a second n-type region 18 to be used as a source is  
 formed at the other side of said shallow p-type region  
 15 in said N-well 14. That is, the doped regions where  
 20 the drain 17 and the source 18 are respectively formed  
 have different conductivity types of dopants.

However, None of Onakado et al., Bergemont, and  
 Komori et al. teach that the doped regions where a drain  
 25 and a source are respectively formed have different  
 conductivity types of dopants. Onakado et al. disclose  
 that the memory cell transistor MC1a includes a drain  
 region 150 formed in an N-type well and a source region  
 154 formed in the N-type well (col. 11, lines 22-34,  
 30 & Fig. 2). Since the drain region 150 and the source  
 region 154 are both formed in the N-type well in the  
 Onakado et al.'s teaching, the memory cell taught in

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the amended claim 1 of the present application should be definitely different from that disclosed in Onakado et al.'s disclosure.

5        Additionally, Bergemont discloses that a flash  
EPROM cell includes an M<sup>+</sup> source bit line 242 formed  
in a P-well 202 and an M<sup>+</sup> drain bit line 242 formed in  
the P-well 202 (col.6, lines 51-60, & Fig.17). That  
is, the source 242 and the drain 242 are both formed  
10    in the P-well 202 in Bergemont's disclosure. Therefore,  
it is believed that the memory cell taught in the amended  
claim 1 of the present application is definitely  
different from that disclosed in Bergemont's  
disclosure.

15        Furthermore, Komori et al. disclose that a memory  
cell of an EPROM includes a source region 16 formed  
in a p-well 5 and a drain region 16 formed in the p-well  
5 (col.5, lines 40-47, & Fig.3). In Komori et al.'s  
20    teaching, the source region 16 and the drain region  
16 are both formed in the p-well 5, so that the memory  
cell taught in the amended claim 1 of the present  
application should be definitely different from that  
disclosed in Komori et al.'s disclosure.

25        Form the above discussion, Onakado et al., Bergemont,  
and Komori et al. never disclose that the doped regions  
where a drain and a source are respectively formed have  
different conductivity types of dopants. Therefore,  
30    it is believed non-obvious to one of ordinary skill  
in the art at the time the invention was made to combine  
Onakado et al., Bergemont, and Komori et al.'s

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disclosures to form the art disclosed in the amended claim 1. Reconsideration of the amended claim 1 is hereby requested.

5 As claims 2, 5-6, and 13-16 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. Reconsideration of the claims 2, 5-6, and 13-16 is hereby requested.

10 5. Rejection of claim 3 under 35 U.S.C. 103(a):

Onakado et al., Bergemont, and Komori et al. are applied as above but fail to expressly disclose wherein a smiling effect pattern is caused by oxidation between said stacked gate and said oxide layer.

15 Heieh et al. disclose using the smiling effect in order to improve the efficiency of a flash memory cell (see abstract). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Onakado et al. modified by Bergemont and Komori et al. so as to cause a smiling effect between the stacked gate and the oxide layer in order to improve programming efficiency.

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**Response:**

As claim 3 is dependent upon the amended claim 1, it should be allowed if the amended claim 1 is allowed. Reconsideration of the claim 3 is hereby requested.

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6. Allowance of claim 4 and 7-8:

Claims 4 and 7-8 are objected to as being dependent

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upon a rejected base claim, but would be allowable if  
rewritten in independent form including all of the  
limitations of the base claim and any intervening  
claims.

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**Response:**

Claims 4 and 7 are canceled because they are emerged  
into the claim 1. Additionally, since claim 7 is canceled,  
claim 8 is amended to be dependent upon the amended  
claim 1. Nor new matter is entered. Allowance of the  
present application is politely requested.

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Sincerely yours,

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